

invention.

What is claimed is:

1. A method of fabricating a titanium disilicide film in  
the manufacture of an integrated circuit comprising:

providing a semiconductor substrate having silicon  
regions to be silicided;

5       depositing a titanium layer overlying said silicon  
regions to be silicided;

subjecting said substrate to a first annealing  
whereby said titanium is transformed to phase C40  
titanium disilicide where it overlies said silicon  
10      regions and wherein said titanium not overlying said  
silicon regions is unreacted;

subjecting said substrate to a second annealing  
whereby phase C54 titanium disilicide is grown overlying  
said phase C40 titanium disilicide and whereby said  
15      phase C40 titanium disilicide is transformed to phase  
C54 titanium disilicide; and

removing said unreacted titanium layer to complete  
formation of said titanium disilicide film in the  
manufacture of said integrated circuit.

2. The method according to Claim 1 wherein said silicon  
regions to be silicided comprise gate electrodes and  
associated source and drain regions.

3. The method according to Claim 1 wherein said titanium layer is sputter deposited to a thickness of between about 100 and 500 Angstroms.
4. The method according to Claim 1 wherein said first annealing is a laser annealing using a laser having a wavelength of 1.06 nm and energy between about 0.5 and 1.5 Joules/cm<sup>2</sup>.
5. The method according to Claim 1 wherein said first annealing is a laser annealing using an Excimer laser having a wavelength of 248 nm and energy between about 0.1 and 1.2 Joules/cm<sup>2</sup>.
6. The method according to Claim 1 wherein said second annealing is a rapid thermal annealing performed at a temperature of between about 550 and 860 °C for 0.5 to 2 minutes.
7. The method according to Claim 1 wherein said second annealing is a furnace annealing performed at a temperature of between about 500 and 750 °C for 5 to 60 minutes.

8. A method of fabricating a titanium disilicide film in the manufacture of an integrated circuit comprising:

providing a semiconductor substrate having silicon regions to be silicided;

5 depositing a titanium layer overlying said silicon regions to be silicided;

subjecting said substrate to a laser annealing whereby said titanium is transformed to phase C40 titanium disilicide where it overlies said silicon 10 regions and wherein said titanium not overlying said silicon regions is unreacted;

subjecting said substrate to a low temperature annealing whereby said phase C40 titanium disilicide is grown overlying said phase C40 titanium disilicide and 15 whereby said phase C40 titanium disilicide is transformed to phase C54 titanium disilicide; and

removing said unreacted titanium layer to complete formation of said titanium disilicide film in the manufacture of said integrated circuit.

9. The method according to Claim 8 wherein said silicon regions to be silicided comprise gate electrodes and associated source and drain regions.

10. The method according to Claim 8 wherein said titanium layer is sputter deposited to a thickness of between about 100 and 500 Angstroms.
11. The method according to Claim 8 wherein said laser annealing uses a laser having a wavelength of 1.06 nm and energy between about 0.5 and 1.5 Joules/cm<sup>2</sup>.
12. The method according to Claim 8 wherein said laser annealing uses an Excimer laser having a wavelength of 248 nm and energy between about 0.1 and 1.2 Joules/cm<sup>2</sup>.
13. The method according to Claim 8 wherein said low temperature annealing is a rapid thermal annealing performed at a temperature of between about 550 and 860 °C for 0.5 to 2 minutes.
14. The method according to Claim 8 wherein said low temperature annealing is a furnace annealing performed at a temperature of between about 500 and 750 °C for 5 to 60 minutes.
15. A method of fabricating a titanium disilicide film in the manufacture of an integrated circuit comprising:  
providing a semiconductor substrate having silicon

regions to be silicided;

5       depositing a titanium layer overlying said silicon  
regions to be silicided;

         subjecting said substrate to a first annealing  
whereby said titanium is transformed to phase C40  
titanium disilicide where it overlies said silicon  
10      regions and wherein said titanium not overlying said  
silicon regions is unreacted;

         subjecting said substrate to a second annealing at  
a temperature of less than 700 °C whereby said phase C40  
titanium disilicide is transformed to phase C54 titanium  
15      disilicide; and

         removing said unreacted titanium disilicide to  
complete formation of said titanium disilicide film in  
the manufacture of said integrated circuit.

16. The method according to Claim 15 wherein said  
silicon regions to be silicided comprise gate electrodes  
and associated source and drain regions.

17. The method according to Claim 15 wherein said  
titanium layer is sputter deposited to a thickness of  
between about 100 and 500 Angstroms.

18. The method according to Claim 15 wherein said first annealing is a laser annealing using a laser having a wavelength of 1.06 nm and energy between about 0.5 and 1.5 Joules/cm<sup>2</sup>.
19. The method according to Claim 15 wherein said first annealing is a laser annealing using an Excimer laser having a wavelength of 248 nm and energy between about 0.1 and 1.2 Joules/cm<sup>2</sup>.
20. The method according to Claim 15 wherein said second annealing is a rapid thermal annealing performed at a temperature of between about 550 and 860 °C for 0.5 to 2 minutes.
21. The method according to Claim 15 wherein said second annealing is a furnace annealing performed at a temperature of between about 500 and 750 °C for 5 to 60 minutes.